Patent Claims

1. Delay control apparatus for provision of clock signals in circuit units, in which the clock signals within the circuit units can be predetermined variably in time with respect to an external clock signal, having:

a) a delay device (100) comprising a first delay element (101) for provision of a variable time delay (105) between an output signal (104) and an input signal (103) for the first delay element (101);

b) a feedback device (106) to which the output signal (104) is supplied, for feeding back the output signal (104), in which the feedback device (106) emits a time-delayed, fed-back output signal (107); and

c) a phase difference detection device (108), to which the input signal (103) and the fed-back output signal (107) are supplied, for detection of a phase difference between the input signal (103) and the fed-back output signal (107), in which the phase difference detection device emits a control signal (109) for controlling the first delay element (101) as a function of the detected phase difference;

characterized
in that the delay control apparatus also has:

d) at least one second delay element (102) which is connected in series with the first delay element (101); and

e) a frequency detection unit (110) for detection of the frequency of the input signal (103), in which the second delay element (102) can be adjusted as a

function of the detected frequency of the input signal (103).

2. Apparatus according to Claim 1, characterized in that the delay control apparatus has a filtering device (111) for filtering the control signal (109) which is emitted from the phase difference detection device (108).

3. Apparatus according to Claim 1, characterized in that the feedback device (106) has a time delay which corresponds to the sum of a receiver time delay (201) and of a driver time delay (203).

4. Apparatus according to Claim 1, characterized in that a second delay element (102) for low frequencies of the input signal (103), and at least one further second delay element (102) for high frequencies of the input signal (103), are provided in the delay device (100).

5. Apparatus according to Claim 1, characterized in that the delay device (100) is formed by at least one capacitor element (305) which is varied by means of a control voltage (304).

6. Apparatus according to Claim 1, characterized in that the delay device (100) is formed by at least one current inverter which is varied by means of a control voltage (304).

7. Apparatus according to Claim 1, characterized

in that the delay device (100) is formed by an inverter chain.

8. Method for provision of clock signals in circuit units, in which the clock signals within the circuit units are predetermined variably in time with respect to an external clock signal, having the following steps:

a) provision of a variable time delay (105) between an output signal (104) and an input signal (103) of a delay device (100) with a first delay element (101);

b) feedback of the output signal (104) by means of a feedback device (106) to which the output signal (104) is supplied, in which the feedback device (106) emits a time-delayed, fed-back output signal (107), and

c) detection of the phase difference between the input signal (103) and the fed-back output signal (107) by means of a phase difference detection device (108) to which the input signal (103) and the fed-back output signal (107) are supplied, in which the phase difference detection device emits a control signal (109) for controlling the first delay element (101) as a function of the detected phase difference;

characterized in that

d) the frequency of the input signal (103) is detected by means of a frequency detection unit (110); and

e) at least one second delay element (102), which is connected in series with the first delay element (101), is adjusted as a function of the detected frequency of the input signal (103).

9. Method according to Claim 8,

characterized
in that in order to allow the frequency detection unit (110) to adjust the time delay of the second delay element (102), the cycle time of the delay control apparatus is compared with a number, which can be predetermined, of delay units (205) for the second delay element (102).

10. Method according to Claim 9,
characterized
in that the number of delay units (205) for the second delay element (102) is eight.

11. Method according to Claim 8,
characterized
in that the delay control apparatus is reset by means of a reset pulse (209) before frequency detection by means of the frequency detection unit (110).

12. Method according to Claim 8,
characterized
in that an overlap area (210) is provided between adjacent detection frequency ranges (211, 212).

13. Method according to Claim 8,
characterized
in that the output signal (104) is delayed by the sum of a receiver time delay (201) and of a driver time delay (203) for feeding back in the feedback device (106), to which the output signal (104) is supplied.

14. Method according to Claim 8,
characterized
in that the control signal (109) which is emitted from the phase difference detection device (108) is filtered in a filtering device (111) for the delay control apparatus.